III AMENDMENTS

AMENDMENTS TO THE CLAIMS

Cancel claims 1-4 and 6-40 as being directed to a non-elected invention and substitute in place thereof claims 59-97 as follows.

--59. A filter processor implemented on a single integrated circuit chip comprising:

an integrated circuit read only memory storing instructions, wherein the integrated circuit read only memory is implemented on the single integrated circuit chip;

an integrated circuit alterable memory storing operands, wherein the integrated circuit alterable memory is implemented on the single integrated circuit chip;

an integrated circuit input circuit coupled to the integrated circuit read only memory and generating input signals in response to the instructions, wherein the integrated circuit input circuit is implemented on the single integrated circuit chip;

an integrated circuit writing circuit coupled to the integrated circuit read only memory, integrated circuit input circuit, and to the integrated circuit alterable memory and writing operands into the integrated circuit alterable memory in response to the input signals and in response to the instructions, wherein the integrated circuit input circuit is implemented on the single integrated circuit chip;

an integrated circuit processing circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and generating filtered operands in response to the operands and in response to the instructions, wherein the integrated circuit processing circuit is implemented on the single integrated circuit chip, and wherein the integrated circuit processing circuit includes;

a) an integrated circuit multiplier circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and generating product operands by multiplying operands in response to the instructions and

b) an integrated circuit adder circuit coupled to the integrated circuit read only memory and generating filtered operands by adding the product operands in response to the instructions; and

an integrated circuit output circuit coupled to the integrated circuit read only memory and generating output operands by outputting the filtered operands in response to the instructions, wherein the integrated circuit output circuit is implemented on the single integrated circuit chip.

--60. A filter processor implemented on a single integrated circuit chip as set forth in claim 59:

wherein the filter processor is a correlator filter processor;

wherein the integrated circuit read only memory stores the instructions as correlator instructions;

wherein the integrated circuit alterable memory stores the operands as correlator operands;

wherein the integrated circuit processing circuit generates the filtered operands as correlation filtered operands in response to the correlator operands and in response to the correlator instructions, and

wherein the integrated circuit output circuit generates the output operands by outputting the correlation filtered operands in response to the instructions.

--61. A filter processor implemented on a single integrated circuit chip as set forth in claim 59, further comprising:

an integrated circuit synchronization circuit generating synchronization signals, wherein the integrated circuit input circuit is implemented on the single integrated circuit chip;

wherein the integrated circuit processing circuit is coupled to the integrated circuit synchronization circuit and further generates the filtered operands in response to the synchronization signal.

--62. A filter processor implemented on a single integrated circuit chip as set forth in claim 59, wherein the integrated circuit processing circuit is an integrated circuit iterative processing circuit iteratively generating the filtered operands.

--63. A filter processor implemented on a single integrated circuit chip as set forth in claim 59, wherein the integrated circuit processing circuit is an integrated circuit multiple loop iterative processing circuit iteratively generating the filtered operands with multiple iterative loops.

--64. A filter processor implemented on a single integrated circuit chip as set forth in claim 59, wherein the integrated circuit alterable memory includes an integrated circuit dynamic random access alterable memory dynamically storing operands, said filter processor further comprising a refresh circuit coupled to the integrated circuit alterable memory and refreshing the integrated circuit alterable memory.

--65. A filter processor implemented on a single integrated circuit chip comprising:

an integrated circuit read only memory storing instructions, wherein the integrated circuit read only memory is implemented on the single integrated circuit chip;

an integrated circuit alterable memory storing operands, wherein the integrated circuit alterable memory is implemented on the single integrated circuit chip;

an integrated circuit input circuit coupled to the integrated circuit read only memory and generating input signal samples in response to the instructions, wherein the integrated circuit input circuit is implemented on the single integrated circuit chip;

an integrated circuit writing circuit coupled to the integrated circuit read only memory, integrated circuit input circuit, and to the integrated circuit alterable memory and writing operands into the integrated circuit alterable memory in response to the input signal samples and in response to the instructions, wherein the integrated circuit input circuit is implemented on the single integrated circuit chip;

an integrated circuit processing circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and generating filtered operands in response to the operands and in response to the instructions, wherein the integrated circuit processing circuit is implemented on the single integrated circuit chip, and wherein the integrated circuit processing circuit includes;

a) an integrated circuit multiplier circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and generating product operands by multiplying operands in response to the instructions and

b) an integrated circuit adder circuit coupled to the integrated circuit read only memory and generating filtered operands by adding the product operands in response to the instructions; and

an integrated circuit output circuit coupled to the integrated circuit read only memory and generating output operands by outputting the filtered operands in response to the instructions, wherein the integrated circuit output circuit is implemented on the single integrated circuit chip.

--66. A filter processor implemented on a single integrated circuit chip as set forth in claim 65:

wherein the filter processor is a correlator filter processor;

wherein the integrated circuit read only memory stores the instructions as correlator instructions;

wherein the integrated circuit alterable memory stores the operands as correlator operands;

wherein the integrated circuit processing circuit generates the filtered operands as correlation filtered operands in response to the correlator operands and in response to the correlator instructions, and

wherein the integrated circuit output circuit generates the output operands by outputting the correlation filtered operands in response to the instructions.

--67. A filter processor implemented on a single integrated circuit chip as set forth in claim 65, further comprising:

an integrated circuit synchronization circuit generating a synchronization signal, wherein the integrated circuit input circuit is implemented on the single integrated circuit chip;

wherein the integrated circuit processing circuit is coupled to the integrated circuit synchronization circuit and further generates the filtered operands in response to the synchronization signal.

--68. A filter processor implemented on a single integrated circuit chip as set forth in claim 65, wherein the integrated circuit processing circuit is an integrated circuit iterative processing circuit iteratively generating the filtered operands.

--69. A filter processor implemented on a single integrated circuit chip as set forth in claim 65, wherein the integrated circuit processing circuit is an integrated circuit multiple loop iterative processing circuit iteratively generating the filtered operands with multiple iterative loops.

--70. A filter processor implemented on a single integrated circuit chip as set forth in claim 65, wherein the integrated circuit alterable memory includes an integrated circuit dynamic random access alterable memory dynamically storing operands, said filter processor further comprising a refresh circuit coupled to the integrated circuit alterable memory and refreshing the integrated circuit alterable memory.

--71. An integrated circuit filter processor comprising:

an integrated circuit read only memory storing instructions;

an integrated circuit alterable memory storing operands;

an integrated circuit input circuit coupled to the integrated circuit read only memory and generating input signals in response to the instructions;

an integrated circuit writing circuit coupled to the integrated circuit read only memory, integrated circuit input circuit, and to the integrated circuit alterable memory and writing operands into the integrated circuit alterable memory in response to the input signals and in response to the instructions;

an integrated circuit processing circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and generating filtered operands in response to

the operands and in response to the instructions, wherein the integrated circuit processing circuit includes;

a) an integrated circuit multiplier circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and generating product operands by multiplying operands in response to the instructions and

b) an integrated circuit adder circuit coupled to the integrated circuit read only memory and generating filtered operands by adding the product operands in response to the instructions; and

an integrated circuit output circuit coupled to the integrated circuit read only memory and generating output operands by outputting the filtered operands in response to the instructions.

--72. An integrated circuit filter processor as set forth in claim 71:

wherein the filter processor is a correlator filter processor;

wherein the integrated circuit read only memory stores the instructions as correlator instructions;

wherein the integrated circuit alterable memory stores the operands as correlator operands;

wherein the integrated circuit processing circuit generates the filtered operands as correlation filtered operands in response to the correlator operands and in response to the correlator instructions, and

wherein the integrated circuit output circuit generates the output operands by outputting the correlation filtered operands in response to the instructions.

--73. An integrated circuit filter processor as set forth in claim 71, further comprising:

an integrated circuit synchronization circuit generating synchronization signals;

wherein the integrated circuit processing circuit is coupled to the integrated circuit synchronization circuit and further generates the filtered operands in response to the synchronization signal.

--74. An integrated circuit filter processor as set forth in claim 71, wherein the integrated circuit processing circuit is an integrated circuit iterative processing circuit iteratively generating the filtered operands.

--75. An integrated circuit filter processor as set forth in claim 71, wherein the integrated circuit processing circuit is an integrated circuit multiple loop iterative processing circuit iteratively generating the filtered operands with multiple iterative loops.

--76. An integrated circuit filter processor as set forth in claim 71, wherein the integrated circuit alterable memory includes an integrated circuit dynamic random access alterable memory dynamically storing operands, said filter processor further comprising a refresh circuit coupled to the integrated circuit alterable memory and refreshing the integrated circuit alterable memory.

--77. An integrated circuit filter processor comprising:

an integrated circuit read only memory storing instructions;

an integrated circuit alterable memory storing operands;

an integrated circuit input circuit coupled to the integrated circuit read only memory and generating input signal samples in response to the instructions;

an integrated circuit writing circuit coupled to the integrated circuit read only memory, integrated circuit input circuit, and to the integrated circuit alterable memory and writing operands into the integrated circuit alterable memory in response to the input signal samples and in response to the instructions;

an integrated circuit processing circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and generating filtered operands in response to the operands and in response to the instructions, and wherein the integrated circuit processing circuit includes;

a) an integrated circuit multiplier circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and generating product operands by multiplying operands in response to the instructions and

b) an integrated circuit adder circuit coupled to the integrated circuit read only memory and generating filtered operands by adding the product operands in response to the instructions; and

an integrated circuit output circuit coupled to the integrated circuit read only memory and generating output operands by outputting the filtered operands in response to the instructions.

--78. An integrated circuit filter processor as set forth in claim 77:

wherein the filter processor is a correlator filter processor;

wherein the integrated circuit read only memory stores the instructions as correlator instructions;

wherein the integrated circuit alterable memory stores the operands as correlator operands;

wherein the integrated circuit processing circuit generates the filtered operands as correlation filtered operands in response to the correlator operands and in response to the correlator instructions, and

wherein the integrated circuit output circuit generates the output operands by outputting the correlation filtered operands in response to the instructions.

--79. An integrated circuit filter processor as set forth in claim 77, further comprising:

an integrated circuit synchronization circuit generating a synchronization signal;

wherein the integrated circuit processing circuit is coupled to the integrated circuit synchronization circuit and further generates the filtered operands in response to the synchronization signal.

--80. An integrated circuit filter processor as set forth in claim 77, wherein the integrated circuit processing circuit is an integrated circuit iterative processing circuit iteratively generating the filtered operands.

--81. An integrated circuit filter processor as set forth in claim 77, wherein the integrated circuit processing circuit is an integrated circuit multiple loop iterative processing circuit iteratively generating the filtered operands with multiple iterative loops.

--82. An integrated circuit filter processor as set forth in claim 77, wherein the integrated circuit alterable memory includes an integrated circuit dynamic random access alterable memory dynamically storing operands, said filter processor further comprising a refresh circuit coupled to the integrated circuit alterable memory and refreshing the integrated circuit alterable memory.

--83. An integrated circuit filter processor comprising:

an integrated circuit read only memory storing instructions;

an integrated circuit dynamic random access memory storing operands;

an integrated circuit input circuit coupled to the integrated circuit read only memory and generating input signals in response to the instructions;

an integrated circuit writing circuit coupled to the integrated circuit read only memory, integrated circuit input circuit, and to the integrated circuit dynamic random access memory and writing operands into the integrated circuit dynamic random access memory in response to the input signals and in response to the instructions;

an integrated circuit processing circuit coupled to the integrated circuit read only memory and to the integrated circuit dynamic random access memory and generating filtered operands in response to the operands and in response to the instructions, wherein the integrated circuit processing circuit includes;

a) an integrated circuit multiplier circuit coupled to the integrated circuit read only memory and to the integrated circuit dynamic random access memory and generating product operands by multiplying operands in response to the instructions and

b) an integrated circuit adder circuit coupled to the integrated circuit read only memory and generating filtered operands by adding the product operands in response to the instructions;

an integrated circuit refresh circuit coupled to the integrated circuit dynamic random access memory and refreshing the integrated circuit dynamic random access memory; and

an integrated circuit output circuit coupled to the integrated circuit read only memory and generating output operands by outputting the filtered operands in response to the instructions.

--84. An integrated circuit filter processor comprising:

an analog to digital converter generating digital converter signals in response to analog input signals;

an integrated circuit read only memory storing instructions;

an integrated circuit dynamic random access memory storing operands;

an integrated circuit input circuit coupled to the integrated circuit read only memory and to the analog to digital converter and generating input signals in response to the instructions and in response to the digital converter signals;

an integrated circuit writing circuit coupled to the integrated circuit read only memory, integrated circuit input circuit, and to the integrated circuit dynamic random access memory and writing operands into the integrated circuit dynamic random access memory in response to the input signals and in response to the instructions;

an integrated circuit processing circuit coupled to the integrated circuit read only memory and to the integrated circuit dynamic random access memory and generating filtered operands in response to the operands and in response to the instructions, wherein the integrated circuit processing circuit includes;

a) an integrated circuit multiplier circuit coupled to the integrated circuit read only memory and to the integrated circuit dynamic random access memory and generating product operands by multiplying operands in response to the instructions and

b) an integrated circuit adder circuit coupled to the integrated circuit read only memory and generating filtered operands by adding

the product operands in response to the instructions;

an integrated circuit refresh circuit coupled to the integrated circuit dynamic random access memory and refreshing the integrated circuit dynamic random access memory; and

an integrated circuit output circuit coupled to the integrated circuit read only memory and generating output operands by outputting the filtered operands in response to the instructions.

--85. An integrated circuit filter processor comprising:

an integrated circuit read only memory storing instructions;

an integrated circuit dynamic random access memory storing operands;

an integrated circuit input circuit coupled to the integrated circuit read only memory and generating input signals in response to the instructions;

an integrated circuit writing circuit coupled to the integrated circuit read only memory, integrated circuit input circuit, and to the integrated circuit dynamic random access memory and writing operands into the integrated circuit dynamic random access memory in response to the input signals and in response to the instructions;

an integrated circuit processing circuit coupled to the integrated circuit read only memory and to the integrated circuit dynamic random access memory and generating filtered operands in response to the operands and in response to the instructions, wherein the integrated circuit processing circuit includes;

a) an integrated circuit multiplier circuit coupled to the integrated circuit read only memory and to the integrated circuit dynamic random access memory and generating product operands by multiplying operands in response to the instructions and

b) an integrated circuit adder circuit coupled to the integrated circuit read only memory and generating filtered operands by adding the product operands in response to the instructions;

an integrated circuit refresh circuit coupled to the integrated circuit dynamic random access memory and refreshing the integrated circuit dynamic random access memory;

an integrated circuit output circuit coupled to the integrated circuit read only memory and generating output operands by outputting the filtered operands in response to the instructions; and

a digital to analog converter coupled to the integrated circuit output circuit and generating an analog output signal in response to the output operands.

--86. An integrated circuit filter processor comprising:

an integrated circuit read only memory storing instructions;

an integrated circuit dynamic random access memory storing operands;

an integrated circuit input circuit coupled to the integrated circuit read only memory and generating input signals in response to the instructions;

an integrated circuit writing circuit coupled to the integrated circuit read only memory, integrated circuit input circuit, and to the integrated circuit dynamic random access memory and writing operands into the integrated circuit dynamic random access memory in response to the input signals and in response to the instructions;

an integrated circuit processing circuit coupled to the integrated circuit read only memory and to the integrated circuit dynamic random access memory and generating filtered operands in response to the operands and in response to the instructions, wherein the integrated circuit processing circuit includes;

a) an integrated circuit multiplier circuit coupled to the integrated circuit read only memory and to the integrated circuit dynamic random access memory and generating product operands by multiplying operands in response to the instructions and

b) an integrated circuit adder circuit coupled to the integrated circuit read only memory and generating filtered operands by adding the product operands in response to the instructions;

an integrated circuit refresh circuit coupled to the integrated circuit dynamic random access memory and refreshing the integrated circuit dynamic random access memory;

an integrated circuit output circuit coupled to the integrated circuit read only memory and generating output operands by outputting the filtered operands in response to the instructions;

a digital to analog converter coupled to the integrated circuit output circuit and generating an analog output signal in response to the output operands; and

a display coupled to the digital to analog converter and displaying information in response to the analog output signal.

--87. An integrated circuit filter processor comprising:

an analog to digital converter generating digital communication signals in response to analog communications input signals;

an integrated circuit read only memory storing instructions;

an integrated circuit alterable memory storing operands;

an integrated circuit input circuit coupled to the integrated circuit read only memory and generating input communications signals in response to the instructions;

an integrated circuit writing circuit coupled to the integrated circuit read only memory, integrated circuit input circuit, and to the integrated circuit alterable memory and writing operands into the integrated circuit alterable memory in response to the input communications signals and in response to the instructions;

an integrated circuit processing circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and generating filtered operands in response to the communications operands and in response to the instructions, wherein the integrated circuit processing circuit includes;

a) an integrated circuit multiplier circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and generating product operands by multiplying communications operands in response to the instructions and

b) an integrated circuit adder circuit coupled to the integrated circuit read only memory and generating filtered operands by adding the product operands in response to the instructions; and

an integrated circuit output circuit coupled to the integrated circuit read only memory and generating output operands by outputting the filtered operands in response to the instructions.

--88. An integrated circuit filter processor as set forth in claim 87:

wherein the filter processor is a correlator filter processor;

wherein the integrated circuit read only memory stores the instructions as correlator instructions;

wherein the integrated circuit alterable memory stores the operands as correlator operands;

wherein the integrated circuit processing circuit generates the filtered operands as correlation filtered operands in response to the correlator operands and in response to the correlator instructions, and

wherein the integrated circuit output circuit generates the output operands by outputting the correlation filtered operands in response to the instructions.

--89. An integrated circuit filter processor as set forth in claim 87, further comprising:

an integrated circuit synchronization circuit generating synchronization signals;

wherein the integrated circuit processing circuit is coupled to the integrated circuit synchronization circuit and further generates the filtered operands in response to the synchronization signal.

--90. An integrated circuit filter processor as set forth in claim 87, wherein the integrated circuit processing circuit is an integrated circuit iterative processing circuit iteratively generating the filtered operands.

--91. An integrated circuit filter processor as set forth in claim 87, wherein the integrated circuit processing circuit is an integrated circuit multiple loop iterative processing circuit iteratively generating the filtered operands with multiple iterative loops.

--92. An integrated circuit filter processor as set forth in claim 87, wherein the integrated circuit alterable memory includes an integrated circuit dynamic random access alterable memory dynamically storing operands, said filter processor further comprising a refresh circuit coupled to the integrated circuit alterable memory and refreshing the integrated circuit alterable memory.

--93. An integrated circuit filter processor as set forth in claim 86,

wherein the filter processor is a correlator filter processor;

wherein the integrated circuit read only memory stores the instructions as correlator instructions;

wherein the integrated circuit alterable memory stores the operands as correlator operands;

wherein the integrated circuit processing circuit generates the filtered operands as correlation filtered operands in response to the correlator operands and in response to the correlator instructions, and

wherein the integrated circuit output circuit generates the output operands by outputting the correlation filtered operands in response to the instructions.

--94. An integrated circuit filter processor as set forth in claim 86, further comprising:

an integrated circuit synchronization circuit generating synchronization signals;

wherein the integrated circuit processing circuit is coupled to the integrated circuit synchronization circuit and further generates the filtered operands in response to the synchronization signal.

--95. An integrated circuit filter processor as set forth in claim 86, wherein the integrated circuit processing circuit is an integrated circuit iterative processing circuit iteratively generating the filtered operands.

--96. An integrated circuit filter processor as set forth in claim 86, wherein the integrated circuit processing circuit is an integrated circuit multiple loop iterative processing circuit iteratively generating the filtered operands with multiple iterative loops.